IN THE CLAIMS

1. (original) A reference voltage adjustment circuit comprising:

a counter circuit for generating a count signal in response to a clock signal;

a decoder circuit for generating a voltage selection signal by decoding the count signal; and

a reference voltage circuit for generating an updated reference voltage in response to the voltage selection signal.

2. (original) The circuit of claim 1 wherein the decoder circuit performs a trim function by outputting a resistance value in response to the count signal.

3. (original) The circuit of claim 1 and further including:

a voltage comparator circuit for generating a disable signal when the updated reference voltage is at least substantially equal to an external reference voltage; and

a count disable circuit for disabling the counter circuit in response to the disable signal.

4. (original) The circuit of claim 3 wherein the count disable circuit comprises a NOR gate coupled to a clock input of the counter circuit, one input of the NOR gate coupled to the disable signal and a second input of the NOR gate coupled to the clock signal.

5. (original) The circuit of claim 2 wherein the trim function comprises:

a plurality of resistors coupled in series; and

a plurality of transistors that bypass a predetermined number of the plurality of resistors in response to the count signal.

6. (original) The circuit of claim 3 and further including a plurality of transmission gates for enabling the external reference voltage and the clock signal in response to a circuit enable signal.

7. (original) The circuit of claim 6 and further including a reset signal generation circuit, coupled to the counter circuit, for generating a reset signal to set the counter circuit to a known state in response to the circuit enable signal.

8. (original) A reference voltage adjustment circuit having an external reference voltage input and an external clock signal input, the circuit comprising:

a counter circuit for generating a count signal in response to an external clock signal on the external clock signal input;

a decoder circuit for decoding the count signal to generate a voltage selection signal;

a reference voltage circuit for generating an updated reference voltage in response to the voltage selection signal;

a comparator circuit coupled to the reference voltage circuit and the external reference voltage input, the comparator circuit generating a count enable/disable signal in response to a comparison between an external reference voltage signal and the updated reference voltage; and

an enable/disable circuit having a first input coupled to the comparator circuit and a second input coupled to the external clock signal input such that the external clock signal is enabled or disabled in response to a state of the count enable/disable signal.

9. (original) The circuit of claim 8 wherein the voltage selection signal is a resistance value generated by at least one resistor in series with a plurality of resistors.

10. (original) The circuit of claim 8 wherein the counter circuit comprises a plurality of master/slave flip-flops each coupled to a fuse latch for latching a first data signal and a corresponding first complementary data signal.

11. (original) The circuit of claim 8 wherein the count signal comprises a plurality of data signals and their respective complementary data signals.

12. (original) The circuit of claim 11 wherein the decoder circuit comprises a plurality of AND functions coupled to the plurality of data signals and the respective complementary data signals.

13. (original) The circuit of claim 8 and further including memory that stores the count signal that is responsible for generating the updated reference signal that is substantially equal to the external reference voltage signal.

14. (original) A reference voltage adjustment circuit having an external reference voltage input and an external clock signal input, the circuit comprising:

a counter circuit for generating a count signal in response to an external clock signal on the external clock signal input;

a decoder circuit for decoding the count signal to generate a desired voltage signal;

a reference voltage circuit for generating an updated reference voltage in response to the desired voltage signal;

a comparator circuit coupled to the reference voltage circuit and the external reference voltage input, the comparator circuit generating a count enable/disable signal in response to a comparison between an external reference voltage signal and the updated reference voltage; and

an enable/disable circuit coupled to the comparator circuit and the external clock signal input such that the external clock signal is enabled or disabled in response to the count enable/disable signal.

15. (original) The circuit of claim 14 and further including:

a first transmission gate coupled between the external reference voltage input and the comparator circuit, the first transmission gate coupled to a circuit enable input such that a circuit enable signal enables the first transmission gate to allow transmission of the external reference voltage signal; and

a second transmission gate coupled between the external clock signal input and the enable/disable circuit, the second transmission gate coupled to the circuit enable signal such that the circuit enable signal enables the second transmission gate to allow transmission of the external clock signal.

16. (original) The circuit of claim 14 and further including a plurality of flash fuse elements coupled to the counter circuit to store the count signal for generating the updated reference voltage that is at least substantially equal to the external reference voltage input.

17. (original) A method for generating a reference voltage comprising:

setting a counter circuit to a known state;

generating a count signal from the counter circuit in response to a clock signal; and

generating an internal reference voltage in response to the clock signal.

18. (original) The method of claim 17 and further including enabling the clock signal in response to a circuit enable signal.

19. (original) The method of claim 17 wherein the count signal comprises four data bits and their complementary data bits.

20. (original) The method of claim 19 wherein the known state is 0000.

21. (original) A method for generating a reference voltage in a reference voltage adjustment circuit, the method comprising:

enabling an external clock signal to the circuit with a circuit enable signal;

enabling an external reference voltage to the circuit with the circuit enable signal;

setting a counter circuit to a known state in response to the circuit enable signal;

generating a count signal from the counter circuit in response to the external clock signal;

generating an internal reference voltage in response to the clock signal;

comparing the internal reference voltage to the external reference voltage; and

if the internal reference voltage is equal to or greater than the external reference voltage, disabling the counter circuit such that the counter circuit stops at a final count signal that generates the internal reference voltage that is greater than or equal to the external reference voltage.

22. (original) The method of claim 21 and further including storing the final count signal in memory elements.

23. (original) A memory device comprising:

a memory array for storing data;

a sense amplifier circuit, coupled to the memory array, for determining a programmed state of portions of the memory array;

a controller circuit that executes memory functions of the memory device; and

a reference voltage adjustment circuit coupled to the sense amplifier circuit for generating an internal reference voltage, the reference voltage adjustment circuit comprising:

a counter circuit for generating a count signal in response to a clock signal;

a decoder circuit for decoding the count signal to generate a voltage selection signal; and

a reference voltage circuit for generating an updated reference voltage in response to the voltage selection signal.

24. (original) An electronic system comprising:

a processor for generating control signals for the electronic system; and

a memory device comprising:

a memory array for storing data;

a sense amplifier circuit, coupled to the memory array, for determining a programmed state of portions of the memory array;

a controller circuit for executing memory functions of the memory device; and

a reference voltage adjustment circuit coupled to the sense amplifier circuit for generating an internal reference voltage, the reference voltage adjustment circuit comprising:

a counter circuit for generating a count signal in response to a clock signal;

a decoder circuit for decoding the count signal to generate a voltage selection signal; and

a reference voltage circuit for generating an updated reference voltage in response to the voltage selection signal.